

ABSTRACT

USE OF SELECTIVE OXIDATION TO FORM ASYMMETRICAL OXIDE FEATURES DURING THE MANUFACTURE OF A SEMICONDUCTOR DEVICE

A sidewall oxidation process for use during the formation of a transistor such as a flash memory cell allows for improved control of a gate oxide profile. The method comprises doping transistor source and drain regions to different doping levels, then performing a transistor sidewall oxidation using a particular process to modify the gate oxide thickness. The oxide forms at a faster rate along the source sidewall than along the drain sidewall. By using ranges within the oxidation environment described, a source side gate oxide having a variable and selectable thickness may be formed, while forming a drain-side oxide which has a single thickness where a thinner layer is desirable. This leads to improved optimization of key competing requirements of a flash memory cell, such as program and erase performance, while maintaining sufficient long-term data retention. The process may allow improved cell scalability, shortened design time, and decreased manufacturing costs.